

Anodic Ta₂O₅ for CMOS Compatible Low Voltage Electrowetting-On-Dielectric Device Fabrication

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Abstract— This paper reports a CMOS compatible fabrication procedure that enables ElectroWetting On Dielectric (EWOD) technology to be post-processed on foundry technology. With driving voltages less than 15V it is believed to be the lowest reported driving voltage for any material system compatible with post-processing on integrated circuits. The process architecture uses anodically grown tantalum pentoxide as the pinhole free high dielectric constant insulator with the overlying 16nm layer of Teflon-AF[®], which provides the hydrophobic surface upon which droplets can be manipulated. This stack provides a very robust dielectric, which maintains a sufficiently high capacitance per unit area for effective operation at the lower voltage favoured by more standard CMOS technology. The paper demonstrates that the sputtered tantalum layer can be integrated with the aluminium (or copper) interconnect of foundry CMOS processes by standard microfabrication techniques.

I. INTRODUCTION

In recent years lab-on-a-chip and bio-MEMS systems, which can manipulate and analyse biological fluidic samples in micro- and nano-litre scales, have emerged as a solution for automating repetitive laboratory tasks [1], [2]. Digital microfluidic devices based on technologies such as dielectrophoresis (DEP), electrowetting on dielectrics (EWOD) and surface acoustic waves (SAW) provide a potentially reconfigurable method of obtaining a bio-MEMS system [2], [3]. Of these, EWOD technology is an attractive option that has a low power consumption making it well suited for the design and manufacture of microfluidic systems [2]. EWOD uses surface tension as a driving force, which can be controlled by applying a suitable voltage to an array of electrodes covered by a two layer dielectric.

A key parameter in EWOD technology is the driving voltage V . The initial work on electrowetting arrays required driving voltages in the range 80-100V [4]. More recently with a more judicious choice of materials, processes and dielectric thickness, the voltage required to manipulate droplets has been reduced below 15V [4]. However, the temperatures required for the deposition of one of these dielectric layers is well in excess of 450°C [5] making the process non-compatible with CMOS post-processing. This paper reports a process architecture that matches the driving voltage of [4] while not involving processing temperatures anywhere near 450°C.

A. Background

The technology of the electrocapillary phenomenon has been extensively described elsewhere [1], and will only be discussed briefly. For an EWOD system, the Young-Lippmann equation describes the wetting angle change for a droplet in terms of the applied voltage V , the relative dielectric constant ϵ_r , the liquid-gas surface tension γ_{lg} and the thickness t of the dielectric:

$$\cos \theta(V) - \cos \theta(0) = \frac{\epsilon_r \epsilon_0}{2\gamma_{lg} t} V^2 \quad (1)$$

Equation (1) identifies the important role played by the dielectric covering the electrodes in determining the driving voltage V required to modify the contact angle θ (40° typically required for droplet movement). From the Young-Lippmann equation, it is clear that in order to reduce the droplet driving voltage, a dielectric with a higher permittivity is required. This is in addition to the requirement for this layer to be totally impervious to the liquid that forms the droplet being manipulated. Failure to meet this latter criterion leads to electrolytic action at the electrode causing the device to cease functioning. Hence, a robust pinhole free dielectric with a sufficiently high breakdown voltage that also acts as a barrier to the liquid is essential for any EWOD device. Finally the dielectric also has to display a hydrophobic surface, which is not normally available with materials meeting the above specifications. As a result, EWOD dielectrics typically consist of two layers; there is the insulating dielectric discussed above and the thin hydrophobic surface layer (e.g. Teflon-AF[®]) that covers it.

B. Large EWOD arrays on a CMOS backplane

Practical, flexible and programmable EWOD systems designed to move, split and merge droplets with predetermined volume, require a large number of electrodes for complex operations. Examples are given in references [2], [6], [7] for sample analysis that use reagent mixing. Obviously each driving electrode in an EWOD device must be individually addressed from a contact pad via interconnect. While the interconnect for single and double rows of electrodes can be simply implemented on a single level of metallisation, this is not the case for arrays with electrode counts of 3×3 or greater. For

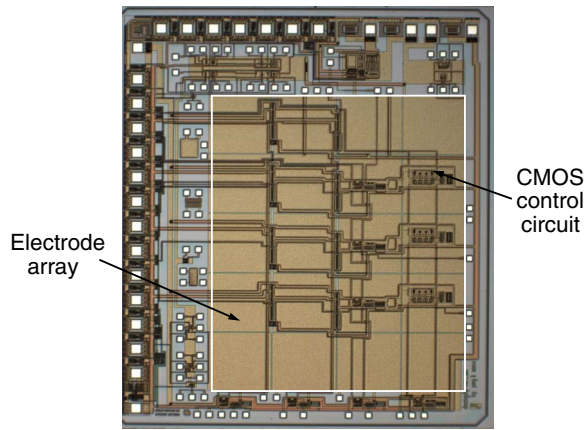


Fig. 1. EWOD electrode array (boxed area) controlled by backplane CMOS circuit [11].

arrays of EWOD electrodes multilevel metallisation is required with the realistic number of electrodes for passive systems being limited by packaging considerations. For example a 30×30 array would require a 900 pin package which is not practical.

Gong et al. partly address the packaging problem by using printed circuit board (PCB) technology together with land grid array (LGA) sockets [7]. The advantage of this solution is its low-cost and system flexibility (i.e., scalable). However, this does not solve the practical aspect of the interconnect problem entirely since a 32×32 digital microfluidic array used in [8] requires over 1000 pins. This is at the limit of a passive electrode drive system and any size bigger really requires an active controlling backplane.

CMOS technology has been widely used for row-column addressing of large numbers of elements, of which the largest application is related to memory devices. Others examples include CMOS imaging chips [9] and micro displays [10]. This approach to addressing arrays obviously lends itself to the realisation of EWOD arrays and, with a large matrix of electrodes, the use of CMOS for backplane row-column addressing enables the utilisation of existing technology. In addition it also makes it possible to provide the electrodes with additional capabilities such as sensing (e.g. pH, temperature, light, voltage etc) and actuation (e.g. temperature control).

Obviously clear advantages exist using on-chip addressing for large two-dimensional arrays. These include a significant reduction in the number of bond pads as well as the simplification of packaging. A dielectrophoresis (DEP) system using a CMOS solution has already been demonstrated [8].

As part of this work an EWOD/CMOS chip has been fabricated and tested [11] (figure 1) using conventional foundry processes and materials. Preparing it for EWOD activation requires post-processing involving the deposition of appropriate dielectric and surface treatment layers.

Previously reported low-voltage EWOD fabrications have used dielectrics deposited at high temperature (e.g. 700°C MOCVD for Barium Strontium Titanate [4], thermal oxida-

tion [12], 700°C annealed BZN ($\text{Bi}_2\text{O}_3 - \text{ZnO} - \text{Nb}_2\text{O}_5$) [13]), none of which are compatible with CMOS technology with aluminium interconnect (deposition temperatures in excess of 450°C are required).

In this work the CMOS foundry process that was used to manufacture the EWOD device employed aluminium at its interconnect. Hence, this determined the electrode metallisation and the passivation layer. For typical foundry processes the passivation is a relatively thick dielectric layer ($0.5 - 1.0 \mu\text{m}$) of silicon dioxide or nitride (or oxynitride), neither of which possesses a very high dielectric constant.

For an effective EWOD implementation using this dielectric technology, a comparatively high operating voltage in the region of 70V is required to drive droplets. This is a direct consequence of the low dielectric constant associated with the passivation layer. Hence the high drive voltage requirement determined the selection of 100V CMOS foundry process for the EWOD backplane. The post-processing and the demonstration of the completed EWOD device is presented in the next section.

Having fabricated and post-processed a high voltage CMOS EWOD device the challenge was to select an improved material system that was fully compatible with EWOD, while at the same time being suitable for integration with a lower voltage CMOS technology. The material system selected is based upon a tantalum pentoxide insulating layer (a high ϵ_r dielectric which can be grown pinhole free), covered by a uniform and thin ($<20\text{nm}$ thick) overlying layer of Teflon-AF[®] to provide the required hydrophobic surface. This material system, which involves no high temperature process, simply consists of Ta/Ta₂O₅/Teflon-AF[®] layers. This is compatible with standard foundry CMOS IC technology for which the metallisation scheme is conventional aluminium interconnect.

II. ANODIC Ta₂O₅ IN LOW VOLTAGE EWOD FOR CMOS INTEGRATION

A. Multilevel metallisation structure

In order to mimic the technology of a standard CMOS chip with aluminium interconnect (figure 2(a)), a two-level aluminium metallisation process was designed and an electrode array fabricated.

Initially, aluminium was used for both metal levels, as in the foundry CMOS chip discussed above. After the top-level metal was patterned it was covered with post-process dielectric layers of vapour deposited Parylene-C[®] and spin coated Teflon-AF[®] (figure 2(b)), both processes being performed at room temperature.

This completes the processing and droplet manipulation for this structure has been achieved using a drive voltage of 80V (figure 3). By applying the same post-processes on the CMOS backplane chip in figure 1, droplet movement was achieved with a drive voltage of 60V as shown in figure 4.

B. Anodic Ta₂O₅ process

Anodically grown tantalum pentoxide is widely used in electrolytic capacitors to provide large area pinhole free di-

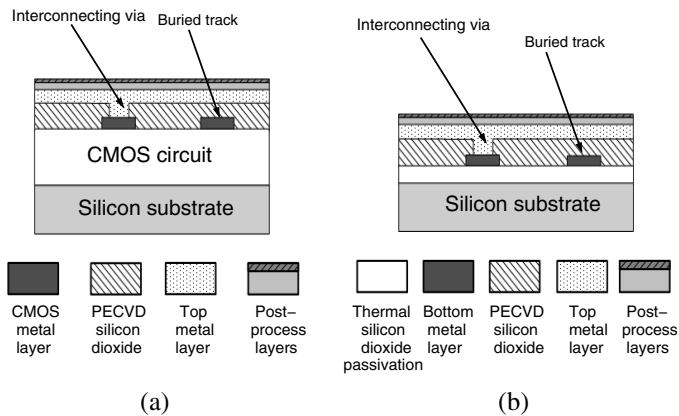


Fig. 2. (a) Cross-section of a CMOS backplane chip and the post-processed layers, (b) cross-section of a two-level metallisation chip representing the CMOS chip and the post-processed layers.

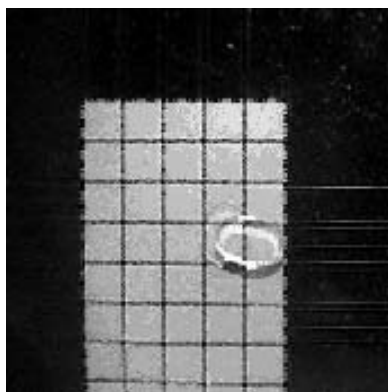


Fig. 3. A moving droplet on a two-level metallisation (aluminium) EWOD chip with a high driving voltage of 80V.

electrics. Ta_2O_5 has a higher ϵ_r (~ 20), than SiO_2 or Si_3N_4 , and in combination with a thin Teflon-AF[®] ($< 20nm$) layer results in a high capacitance, which reduces the driving voltage to less than 15V. The low temperature process associated with the EWOD dielectric sandwich allows it to be post-processed on top of standard CMOS foundry technology.

To demonstrate the Ta_2O_5 -Teflon-AF[®] dielectric system the top aluminium layer in figure 2(b) was replaced by sputtered tantalum and patterned using the same mask. Tantalum can be etched in fluorine-containing plasmas such as CF_4 , SF_6 , CF_3Cl with CH_3F , sometimes mixed with O_2 [14], [15]. The drawback is that these processes will potentially attack any

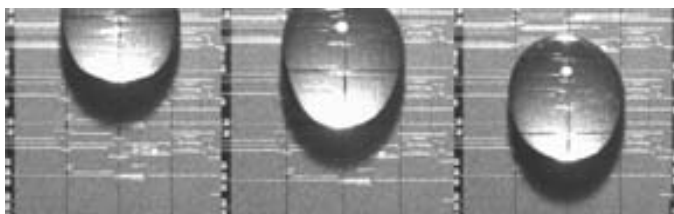


Fig. 4. A moving droplet (3 frames, left to right) on post-processed EWOD electrode array controlled by CMOS backplane.

underlying PECVD SiO_2 layer, which may be problematic if the tantalum etching is not uniform.

By using $SiCl_4$ mixed with NF_3 plasma, Shimada et al. obtained an etch selectivity greater than 80:1 between tantalum and SiO_2 (10:1 in absence of NF_3) [16].

An alternative is XeF_2 dry etching, which is commonly used for silicon etch release in MEMS fabrication, especially post-CMOS etch release due to its high selectivity to other materials (greater than 1000:1 for silicon to SiO_2 and aluminium) [17]. It has also been observed to rapidly etch tantalum as well. The etch process was evaluated using a Memstar[®] tool and no aluminium or SiO_2 attack was observed. The only potential issue is the degree of undercut with an average value of $3.0\mu m$ on each side being measured when etching $0.45\mu m$ thick tantalum. As the gap between EWOD electrodes in this case is $30\mu m$, this undercut rate is acceptable and if need be, could be accounted for by a bias in the mask.

After patterning, the tantalum electrodes are anodised with a gel form citric acid solution. The anodising voltage is applied to every electrode on the chip through the EWOD control circuit in same manner as required for droplet manipulation.

The electrode control system consists of a PC digital I/O card controlled by a C program. The 5V TTL digital outputs are optically isolated from the drive transistors which switch the drive voltage to any combination of electrodes under program control. This drive voltage can be set to any value between 0 and 100V.

After anodisation a thin Teflon-AF[®] layer is deposited using a standard spin coater on the oxidised tantalum electrodes. The measured surface roughness of the anodic Ta_2O_5 has been measured to have a mean roughness R_a between 0.4 to 0.6nm with the Teflon-AF[®] layer thickness uniformity across the wafer within 10%.

The resulting EWOD array is a two-level metallisation structure which has aluminium as the bottom metal with tantalum as the second (top) metal electrode. A 50V anodisation voltage was used resulting in 95nm of Ta_2O_5 . This was followed by a 0.3% Teflon-AF[®] (diluted in Fluorinert solvent FC-75) being spin coated at 2000 rpm for 50 sec, giving 16nm of Teflon-AF[®].

III. EXPERIMENT AND RESULTS

A common two-plate configuration EWOD chip [18] with asymmetric electrode arrangement has been used in the experiments to evaluate the Ta_2O_5 /Teflon-AF[®] system. A conductive indium tin oxide (ITO) covered glass plate coated with 20nm Teflon-AF[®] was placed above the EWOD electrode array. Spacers were used to define the distance between the plates and hence the height of droplets. In this case the spacers were 258 microns.

This combination of dielectric materials on the EWOD device (95nm Ta_2O_5 and 16nm of Teflon-AF[®]) enabled deionized water to move at 14V, with a speed of $2mm \cdot s^{-1}$ (shown in figure 5).

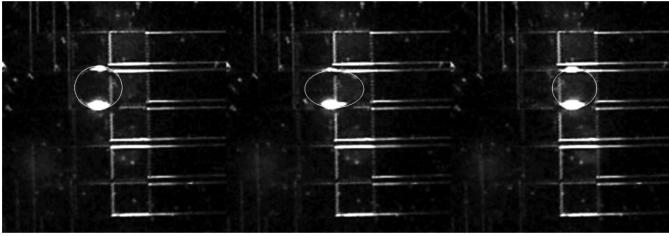


Fig. 5. Three frames (left to right) showing a moving droplet on a two-level metallisation EWOD chip coated with 95nm Ta₂O₅ and 16nm Teflon-AF[®] (the outlines of the droplet have been enhanced for clarity).

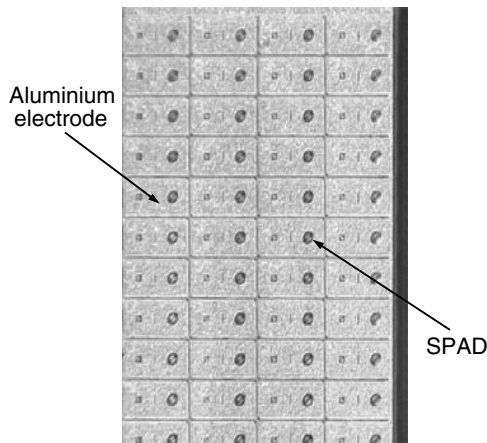


Fig. 6. A prototype design of an EWOD array with electrodes integrated with SPAD (Single Photon Avalanche Diodes) [19].

IV. CONCLUSION

This paper has described what is believed to be the first fully CMOS compatible EWOD system that can drive liquid droplets using voltages less than 15V. The method of producing a thin uniform film of high permittivity dielectric by the anodisation of tantalum, together with a reliable method of spinning thin uniform Teflon-AF[®] films, are the keys to achieving the required low operating potential. The resulting system, with its robust and pinhole free anodised Ta₂O₅, provides a high dielectric constant and an impervious barrier to the liquids being transported, which is not always the case with deposited dielectrics.

In addition an EWOD post-process foundry CMOS chip has been processed and droplet movement demonstrated. The next step is to significantly increase the number of electrodes so that it becomes possible to implement a programmable electrode array size and start integrating further functionality into the electrodes. Figure 6 shows part of a prototype design that provides an example of both of these elements. It consists of an EWOD array with 200µm×100µm electrodes integrated with SPAD (Single Photon Avalanche Diodes) for light detection and this gives one example of the direction digital microfluidics will be moving in the future.

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